



32Mx64 bits Unbuffered DDR SDRAM DIMM

HYMD232646C8J

DESCRIPTION

PRELIMINARY

Hynix HYMD232646C8J series is unbuffered 184-pin double data rate Synchronous DRAM Dual In-Line Memory Modules(DIMMs) which are organized as 32Mx64 high-speed memory arrays. Hynix HYMD232646C8J series consists of eight 32Mx8 DDR SDRAM in 400mil TSOP II packages on a 184pin glass-epoxy substrate. Hynix HYMD232646C8J series provide a high performance 8-byte interface in 5.25" width form factor of industry standard. It is suitable for easy interchange and addition.

Hynix HYMD232646C8J series is designed for high speed of up to 200MHz and offers fully synchronous operations referenced to both rising and falling edges of differential clock inputs. While all addresses and control inputs are latched on the rising edges of the clock, Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL_2. High speed frequencies, programmable latencies and burst lengths allow variety of device operation in high performance memory system.

Hynix HYMD232646C8J series incorporates SPD(serial presence detect). Serial presence detect function is implemented via a serial 2,048-bit EEPROM. The first 128 bytes of serial PD data are programmed by Hynix to identify DIMM type, capacity and other the information of DIMM and the last 128 bytes are available to the customer.

FEATURES

- 256MB (32M x 64) Unbuffered DDR DIMM based on 32Mx8 DDR SDRAM
- JEDEC Standard 184-pin dual in-line memory module (DIMM)
- 2.5V +/- 0.2V VDD and VDDQ Power supply
- 2.6V +/- 0.1V VDD and VDDQ Power supply for DDR400
- All inputs and outputs are compatible with SSTL_2 interface
- Fully differential clock operations (CK & /CK) with 125MHz/133MHz/166MHz/200MHz
- All addresses and control inputs except Data, Data strobes and Data masks latched on the rising edges of the clock
- Data(DQ), Data strobes and Write masks latched on both rising and falling edges of the clock
- Data inputs on DQS centers when write (centered DQ)
- Data strobes synchronized with output data for read and input data for write
- Programmable CAS Latency 3/ 2 / 2.5 supported
- Programmable Burst Length 2 / 4 / 8 with both sequential and interleave mode
- tRAS Lock-out function supported
- Internal four bank operations with single pulsed RAS
- Auto refresh and self refresh supported
- 8192 refresh cycles / 64ms

ORDERING INFORMATION

| Part No. | Power Supply | Clock Frequency | Interface | Form Factor |
|-------------------|---------------|-----------------|-----------|---|
| HYMD232646C8J-J | VDD=VDDQ=2.5V | 166MHz (DDR333) | SSTL_2 | 184pin Unbuffered DIMM 5.25 x 1.25 x 0.15 inch |
| HYMD232646C8J-D4 | VDD=VDDQ=2.6V | 200MHz (DDR400) | SSTL_2 | 184pin Unbuffered DIMM 5.25 x 1.25 x 0.15 inch |
| HYMD232646C8J-D43 | VDD=VDDQ=2.6V | 200MHz (DDR400) | SSTL_2 | 184pin Unbuffered DIMM 5.25 x 1.25 x 0.15 inch |

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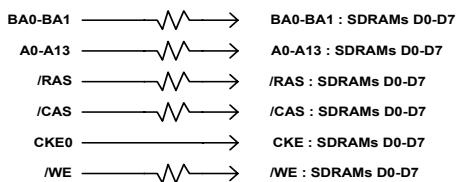
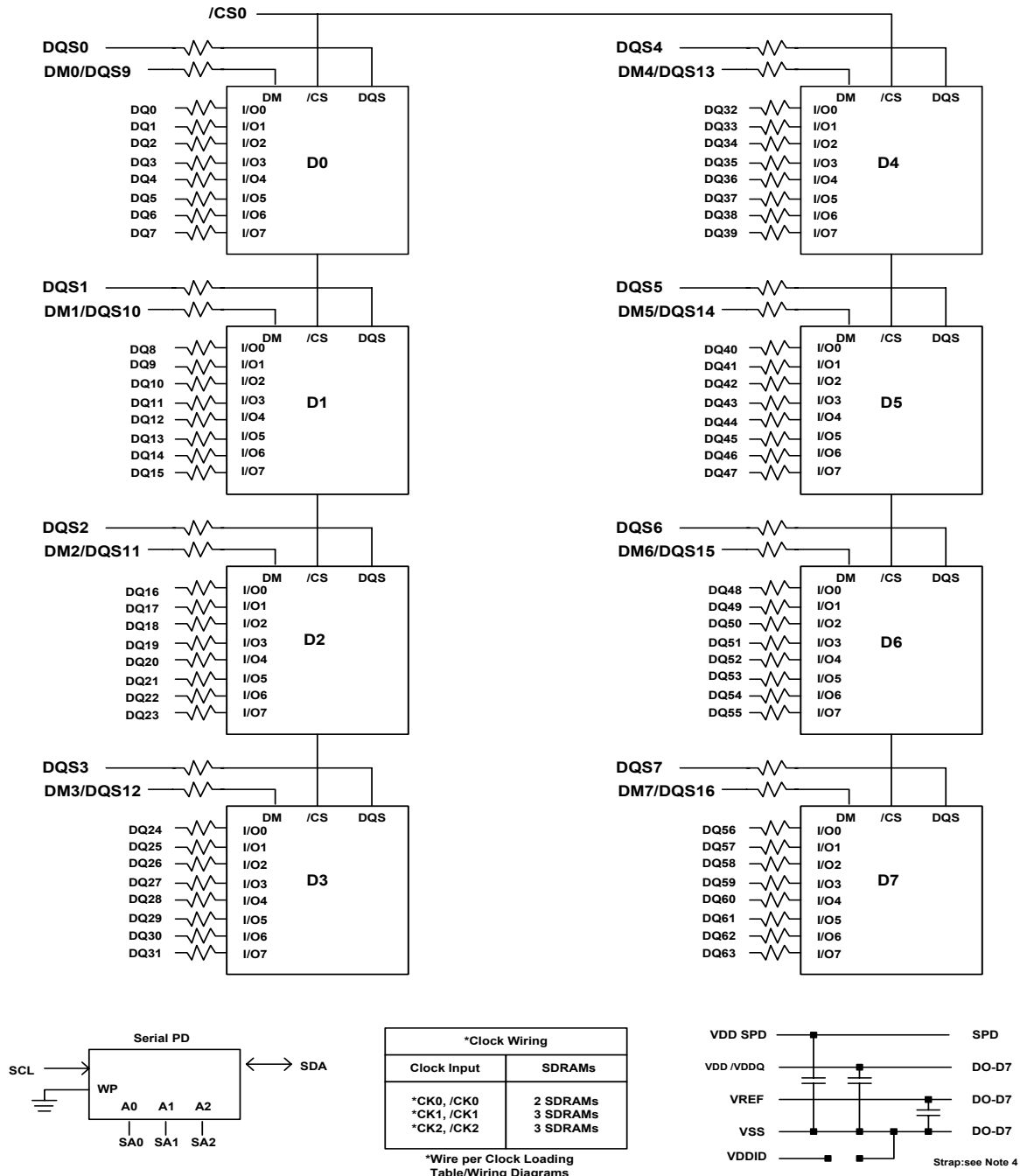
PIN DESCRIPTION

| Pin | Pin Description | Pin | Pin Description |
|----------------------------|----------------------------|---------|------------------------------------|
| CK0,/CK0,CK1,/CK1,CK2,/CK2 | Differential Clock Inputs | VDDQ | DQs Power Supply |
| CS0 | Chip Select Input | VSS | Ground |
| CKE0 | Clock Enable Input | VREF | Reference Power Supply |
| /RAS, /CAS, /WE | Command Sets Inputs | VDDSPD | Power Supply for SPD |
| A0 ~ A12 | Address | SA0~SA2 | E ² PROM Address Inputs |
| BA0, BA1 | Bank Address | SCL | E ² PROM Clock |
| DQ0~DQ63 | Data Inputs/Outputs | SDA | E ² PROM Data I/O |
| DQS0~DQS7 | Data Strobe Inputs/Outputs | VDDID | VDD Identification Flag |
| DM0~DM7 | Data-in Mask | DU | Do not Use |
| VDD | Power Supply | NC | No Connection |

PIN ASSIGNMENT

| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
|-----|------|-----|-------|-----|-------|-----|------|-----|------|-----|--------|
| 1 | VREF | 32 | A5 | 62 | VDDQ | 93 | VSS | 124 | VSS | 154 | /RAS |
| 2 | DQ0 | 33 | DQ24 | 63 | /WE | 94 | DQ4 | 125 | A6 | 155 | DQ45 |
| 3 | VSS | 34 | VSS | 64 | DQ41 | 95 | DQ5 | 126 | DQ28 | 156 | VDDQ |
| 4 | DQ1 | 35 | DQ25 | 65 | /CAS | 96 | VDDQ | 127 | DQ29 | 157 | /CS0 |
| 5 | DQS0 | 36 | DQS3 | 66 | VSS | 97 | DM0 | 128 | VDDQ | 158 | /CS1 |
| 6 | DQ2 | 37 | A4 | 67 | DQS5 | 98 | DQ6 | 129 | DM3 | 159 | DM5 |
| 7 | VDD | 38 | VDD | 68 | DQ42 | 99 | DQ7 | 130 | A3 | 160 | VSS |
| 8 | DQ3 | 39 | DQ26 | 69 | DQ43 | 100 | VSS | 131 | DQ30 | 161 | DQ46 |
| 9 | NC | 40 | DQ27 | 70 | VDD | 101 | NC | 132 | VSS | 162 | DQ47 |
| 10 | NC | 41 | A2 | 71 | NC | 102 | NC | 133 | DQ31 | 163 | NC |
| 11 | VSS | 42 | Vss | 72 | DQ48 | 103 | A13* | 134 | CB4* | 164 | VDDQ |
| 12 | DQ8 | 43 | A1 | 73 | DQ49 | 104 | VDDQ | 135 | CB5* | 165 | DQ52 |
| 13 | DQ9 | 44 | CB0* | 74 | VSS | 105 | DQ12 | 136 | VDDQ | 166 | DQ53 |
| 14 | DQS1 | 45 | CB1* | 75 | /CK2 | 106 | DQ13 | 137 | CK0 | 167 | NC |
| 15 | VDDQ | 46 | VDD | 76 | CK2 | 107 | DM1 | 138 | /CK0 | 168 | VDD |
| 16 | CK1 | 47 | DQS8* | 77 | VDDQ | 108 | VDD | 139 | VSS | 169 | DM6 |
| 17 | /CK1 | 48 | A0 | 78 | DQS6 | 109 | DQ14 | 140 | DM8* | 170 | DQ54 |
| 18 | VSS | 49 | CB2* | 79 | DQ50 | 110 | DQ15 | 141 | A10 | 171 | DQ55 |
| 19 | DQ10 | 50 | VSS | 80 | DQ51 | 111 | CKE1 | 142 | CB6* | 172 | VDDQ |
| 20 | DQ11 | 51 | CB3* | 81 | VSS | 112 | VDDQ | 143 | VDDQ | 173 | NC |
| 21 | CKE0 | 52 | BA1 | 82 | VDDID | 113 | BA2* | 144 | CB7* | 174 | DQ60 |
| 22 | VDDQ | Key | | 83 | DQ56 | 114 | DQ20 | key | | 175 | DQ61 |
| 23 | DQ16 | 53 | DQ32 | 84 | DQ57 | 115 | A12 | 145 | VSS | 176 | VSS |
| 24 | DQ17 | 54 | VDDQ | 85 | VDD | 116 | VSS | 146 | DQ36 | 177 | DM7 |
| 25 | DQS2 | 55 | DQ33 | 86 | DQS7 | 117 | DQ21 | 147 | DQ37 | 178 | DQ62 |
| 26 | VSS | 56 | DQS4 | 87 | DQ58 | 118 | A11 | 148 | VDD | 179 | DQ63 |
| 27 | A9 | 57 | DQ34 | 88 | DQ59 | 119 | DM2 | 149 | DM4 | 180 | VDDQ |
| 28 | DQ18 | 58 | VSS | 89 | VSS | 120 | VDD | 150 | DQ38 | 181 | SA0 |
| 29 | A7 | 59 | BA0 | 90 | WP | 121 | DQ22 | 151 | DQ39 | 182 | SA1 |
| 30 | VDDQ | 60 | DQ35 | 91 | SDA | 122 | A8 | 152 | VSS | 183 | SA2 |
| 31 | DQ19 | 61 | DQ40 | 92 | SCL | 123 | DQ23 | 153 | DQ44 | 184 | VDDSPD |

* These are not used on this module but may be used for other module in 184pin DIMM family

FUNCTIONAL BLOCK DIAGRAM

Note :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors : 22 Ohms ± 5%.
4. VDDID strap connections (for memory device VDD, VDDQ):
 STRAP OUT (OPEN) : VDD = VDDQ
 STRAP IN (VSS) : VDD ≠ VDDQ
5. BAx, Ax, RAS, CAS, WE resistors : 5.1 Ohms ± 5%

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | Unit |
|-------------------------------------|---------|------------|----------|
| Ambient Temperature | TA | 0 ~ 70 | °C |
| Storage Temperature | TSTG | -55 ~ 125 | °C |
| Voltage on Inputs relative to VSS | VIN | -0.5 ~ 3.6 | V |
| Voltage on I/O Pins relative to VSS | VIO | -0.5 ~ 3.6 | V |
| Voltage on VDD relative to VSS | VDD | -0.5 ~ 3.6 | V |
| Voltage on VDDQ relative to VSS | VDDQ | -0.5 ~ 3.6 | V |
| Output Short Circuit Current | IOS | 50 | mA |
| Power Dissipation | PD | 8 | W |
| Soldering Temperature & Time | TSOLDER | 260 / 10 | °C / Sec |

Note : Operation at above absolute maximum rating can adversely affect device reliability

DC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS= 0V)

| Parameter | Symbol | Min | Typ. | Max | Unit | Note |
|----------------------|--------|-------------|----------|-------------|------|------|
| Power Supply Voltage | VDD | 2.3 | 2.5 | 2.7 | V | |
| Power Supply Voltage | VDD | 2.5 | 2.6 | 2.7 | V | 4 |
| Power Supply Voltage | VDDQ | 2.3 | 2.5 | 2.7 | V | 1 |
| Power Supply Voltage | VDDQ | 2.5 | 2.6 | 2.7 | V | 1,4 |
| Input High Voltage | VIH | VREF + 0.15 | - | VDDQ + 0.3 | V | |
| Input Low Voltage | VIL | -0.3 | - | VREF - 0.15 | V | 2 |
| Termination Voltage | VTT | VREF - 0.04 | VREF | VREF + 0.04 | V | |
| Reference Voltage | VREF | 0.49*VDDQ | 0.5*VDDQ | 0.51*VDDQ | V | 3 |

Note :

1. VDDQ must not exceed the level of VDD.
2. VIL (min) is acceptable -1.5V AC pulse width with ≤ 5 ns of duration.
3. The value of VREF is approximately equal to 0.5VDDQ.
4. For DDR400, VDD=2.6V +/- 0.1V, VDDQ=2.6V+/-0.1V

AC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

| Parameter | Symbol | Min | Max | Unit | Note |
|--|---------------------|--------------|--------------|------|------|
| Input High (Logic 1) Voltage, DQ, DQS and DM signals | V _{IH(AC)} | VREF + 0.31 | | V | |
| Input Low (Logic 0) Voltage, DQ, DQS and DM signals | V _{IL(AC)} | | VREF - 0.31 | V | |
| Input Differential Voltage, CK and /CK inputs | V _{ID(AC)} | 0.7 | VDDQ + 0.6 | V | 1 |
| Input Crossing Point Voltage, CK and /CK inputs | V _{IX(AC)} | 0.5*VDDQ-0.2 | 0.5*VDDQ+0.2 | V | 2 |

Note :

1. VID is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of VIX is expected to equal 0.5*V DDQ of the transmitting device and must track variations in the DC level of the same.

AC OPERATING TEST CONDITIONS (TA=0 to 70°C, Voltage referenced to VSS = 0V)

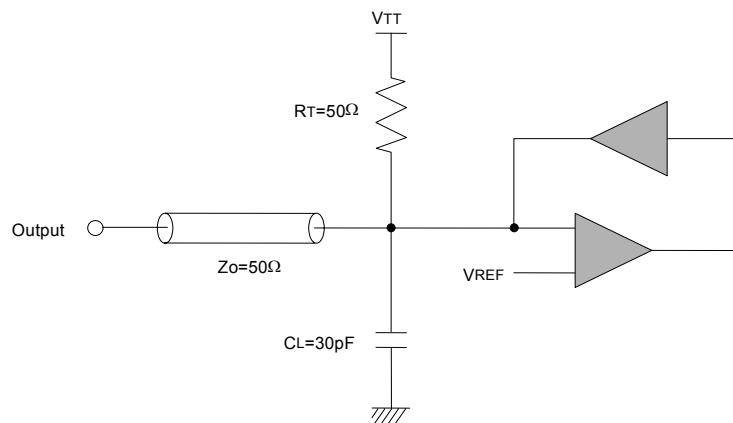
| Parameter | Value | Unit |
|--|-------------|------|
| Reference Voltage | VDDQ x 0.5 | V |
| Termination Voltage | VDDQ x 0.5 | V |
| AC Input High Level Voltage (V _{IH} , min) | VREF + 0.31 | V |
| AC Input Low Level Voltage (V _{IL} , max) | VREF - 0.31 | V |
| Input Timing Measurement Reference Level Voltage | VREF | V |
| Output Timing Measurement Reference Level Voltage | VTT | V |
| Input Signal maximum peak swing | 1.5 | V |
| Input minimum Signal Slew Rate | 1 | V/ns |
| Termination Resistor (RT) | 50 | W |
| Series Resistor (RS) | 25 | W |
| Output Load Capacitance for Access Time Measurement (CL) | 30 | pF |

CAPACITANCE ($T_A=25^\circ\text{C}$, $f=100\text{MHz}$)

| Parameter | Pin | Symbol | Min | Max | Unit |
|---------------------------------|---------------------------------|--------|------|-----|------|
| Input Capacitance | A0 ~ A12, BA0, BA1 | CIN1 | 58 | 72 | pF |
| Input Capacitance | /RAS, /CAS, /WE | CIN2 | 58 | 72 | pF |
| Input Capacitance | CKE0 | CIN3 | 58 | 72 | pF |
| Input Capacitance | CS0 | CIN4 | 58 | 72 | pF |
| Input Capacitance | CK0, /CK0, CK1, /CK1, CK2, /CK2 | CIN5 | 25 | 40 | pF |
| Input Capacitance | DM0 ~ DM7 | CIN6 | 8 | 12 | pF |
| Data Input / Output Capacitance | DQ0 ~ DQ63, DQS0 ~ DQS7 | CIO1 | 7.89 | 12 | pF |

Note :

1. VDD = min. to max., VDDQ = 2.3V to 2.7V, VODC = VDDQ/2, $V_{\text{Opeak-to-peak}} = 0.2\text{V}$
2. Pins not under test are tied to GND.
3. These values are guaranteed by design and are tested on a sample basis only.

OUTPUT LOAD CIRCUIT


DC CHARACTERISTICS I (TA=0 to 70°C, Voltage referenced to VSS = 0V)

| Parameter | | Symbol | Min. | Max | Unit | Note |
|------------------------|---------------------|--------|------------|------------|------|---------------|
| Input Leakage Current | Add, CMD, /CS, /CKE | ILI | -16 | 16 | uA | 1 |
| | CK, /CK | | -12 | 12 | | |
| Output Leakage Current | | ILO | -5 | 5 | uA | 2 |
| Output High Voltage | | VOH | VTT + 0.76 | - | V | IOH = -15.2mA |
| Output Low Voltage | | VOL | - | VTT - 0.76 | V | IOL = +15.2mA |

Note :

1. VIN = 0 to 3.6V, All other pins are not tested under VIN =0V
2. DOUT is disabled, VOUT=0 to 2.7V

DC CHARACTERISTICS II (TA=0 to 70°C, Voltage referenced to VSS = 0V)

| Parameter | Symbol | Test Condition | Speed | | | Unit | Note |
|---|--------|---|-----------|-----|------|------|------|
| | | | D43 | D4 | -J | | |
| Operating Current | IDD0 | One bank; Active Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle | TBD | | 840 | mA | |
| Operating Current | IDD1 | One bank; Active - Read Precharge; Burst Length =2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle | TBD | | 1200 | mA | |
| Precharge Power Down Standby Current | IDD2P | All banks idle; Power down mode; CKE=Low, tCK=tCK(min) | TBD | | 160 | mA | |
| Idle Standby Current | IDD2F | /CS=High, All banks idle ; tCK=tCK(min); CKE=High; address and control inputs changing once per clock cycle. VIN=VREF for DQ, DQS and DM | TBD | | 400 | mA | |
| Active Power Down Standby Current | IDD3P | One bank active; Power down mode; CKE=Low, tCK=tCK(min) | TBD | | 200 | mA | |
| Active Standby Current | IDD3N | /CS=HIGH; CKE=HIGH; One bank; Active Precharge; tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle | TBD | | 480 | mA | |
| Operating Current | IDD4R | Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOU=0mA | TBD | | 2320 | mA | |
| Operating Current | IDD4W | Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM, and DQS inputs changing twice per clock cycle | TBD | | 2320 | | |
| Auto Refresh Current | IDD5 | tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh | TBD | | 1840 | | |
| Self Refresh Current | IDD6 | CKE=<0.2V; External clock on; tCK=tCK(min) | Normal | TBD | 24 | mA | |
| | | | Low Power | TBD | 12 | mA | |
| Operating Current - Four Bank Operation | IDD7 | Four bank interleaving with BL=4 Refer to the following page for detailed test condition | TBD | | 2520 | mA | |

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

| Parameter | Symbol | DDR333 | | Unit | Note | |
|--|--------|-------------------------------------|------|------|---------|--|
| | | Min | Max | | | |
| Row Cycle Time | tRC | 60 | - | ns | | |
| Auto Refresh Row Cycle Time | tRFC | 72 | - | ns | | |
| Row Active Time | tRAS | 42 | 70K | ns | | |
| Active to Read with Auto Precharge Delay | tRAP | 18 | - | ns | 16 | |
| Row Address to Column Address Delay | tRCD | 18 | - | ns | | |
| Row Active to Row Active Delay | tRRD | 12 | - | ns | | |
| Column Address to Column Address Delay | tCCD | 1 | - | CK | | |
| Row Precharge Time | tRP | 18 | - | ns | | |
| Write Recovery Time | tWR | 15 | - | ns | | |
| Last Data-In to Read Command | tDRL | 1 | - | CK | | |
| Auto Precharge Write Recovery + Precharge Time | tDAL | $\frac{tWR}{tCK} + \frac{tRP}{tCK}$ | - | CK | 15 | |
| System Clock Cycle Time | tCK | CL = 2.5 | 6 | 12 | ns | |
| | | CL = 2 | 7.5 | 12 | ns | |
| Clock High Level Width | tCH | 0.45 | 0.55 | CK | | |
| Clock Low Level Width | tCL | 0.45 | 0.55 | CK | | |
| Data-Out edge to Clock edge Skew | tAC | -0.7 | 0.7 | ns | | |
| DQS-Out edge to Clock edge Skew | tDQSCK | -0.6 | 0.6 | ns | | |
| DQS-Out edge to Data-Out edge Skew | tDQSQ | - | 0.45 | ns | | |
| Data-Out hold time from DQS | tQH | tHP -tQHS | - | ns | 1, 10 | |
| Clock Half Period | tHP | min (tCL,tCH) | - | ns | 1,9 | |
| Data Hold Skew Factor | tQHS | - | 0.55 | ns | 10 | |
| Valid Data Output Window | tDV | tQH-tDQSQ | | ns | | |
| Data-out high-impedance window from CK, /CK | tHZ | -0.7 | 0.7 | ns | 17 | |
| Data-out low-impedance window from CK, /CK | tLZ | -0.7 | 0.7 | ns | 17 | |
| Input Setup Time (fast slew rate) | tIS | 0.75 | - | ns | 2,3,5,6 | |
| Input Hold Time (fast slew rate) | tIH | 0.75 | - | ns | 2,3,5,6 | |
| Input Setup Time (slow slew rate) | tIS | 0.8 | - | ns | 2,4,5,6 | |
| Input Hold Time (slow slew rate) | tIH | 0.8 | - | ns | 2,4,5,6 | |

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

- continued -

| Parameter | Symbol | DDR333 | | Unit | Note |
|--|--------|--------|------|------|------------|
| | | Min | Max | | |
| Input Pulse Width | tIPW | 2.2 | | ns | 6 |
| Write DQS High Level Width | tDQSH | 0.35 | - | CK | |
| Write DQS Low Level Width | tDQSL | 0.35 | - | CK | |
| Clock to First Rising edge of DQS-In | tDQSS | 0.75 | 1.25 | CK | |
| Data-In Setup Time to DQS-In (DQ & DM) | tDS | 0.45 | - | ns | 6,7, 11~13 |
| Data-in Hold Time to DQS-In (DQ & DM) | tDH | 0.45 | - | ns | 6,7, 11~13 |
| DQ & DM Input Pulse Width | tDIPW | 1.75 | - | ns | |
| Read DQS Preamble Time | tRPRE | 0.9 | 1.1 | CK | |
| Read DQS Postamble Time | tRPST | 0.4 | 0.6 | CK | |
| Write DQS Preamble Setup Time | tWPRES | 0 | - | CK | |
| Write DQS Preamble Hold Time | tWPREH | 0.25 | - | CK | |
| Write DQS Postamble Time | tWPST | 0.4 | 0.6 | CK | |
| Mode Register Set Delay | tMRD | 2 | - | CK | |
| Exit Self Refresh to Any Execute Command | tXSC | 200 | - | CK | 8 |
| Average Periodic Refresh Interval | tREFI | - | 7.8 | us | |

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

| Parameter | Symbol | DDR400 (D4) | | DDR400 (D43) | | Unit | Note | |
|--|--------|-----------------------|----------|-----------------------|----------|------|---------|--|
| | | Min | Max | Min | Max | | | |
| Row Cycle Time | tRC | 58 | - | 55 | - | ns | | |
| Auto Refresh Row Cycle Time | tRFC | 70 | - | 70 | - | ns | | |
| Row Active Time | tRAS | 40 | 70K | 40 | 70K | ns | | |
| Active to Read with Auto Precharge Delay | tRAP | tRCD or tRAS(min) | - | tRCD or tRAS(min) | - | ns | 16 | |
| Row Address to Column Address Delay | tRCD | 18 | - | 15 | - | ns | | |
| Row Active to Row Active Delay | tRRD | 10 | - | 10 | - | ns | | |
| Column Address to Column Address Delay | tCCD | 1 | - | 1 | - | CK | | |
| Row Precharge Time | tRP | 18 | - | 15 | - | ns | | |
| Write Recovery Time | tWR | 15 | - | 15 | - | ns | | |
| Write to Read Command Delay | tWTR | 2 | - | 2 | - | CK | | |
| Auto Precharge Write Recovery + Precharge Time | tDAL | (tWR/tCK) + (tRP/tCK) | - | (tWR/tCK) + (tRP/tCK) | - | CK | 15 | |
| System Clock Cycle Time | CL = 3 | tCK | 5 | 10 | 5 | 10 | ns | |
| Clock High Level Width | tCH | 0.45 | 0.55 | 0.45 | 0.55 | CK | | |
| Clock Low Level Width | tCL | 0.45 | 0.55 | 0.45 | 0.55 | CK | | |
| Data-Out edge to Clock edge Skew | tAC | -0.7 | 0.7 | -0.7 | 0.7 | ns | | |
| DQS-Out edge to Clock edge Skew | tDQSCK | -0.55 | 0.55 | -0.55 | 0.55 | ns | | |
| DQS-Out edge to Data-Out edge Skew | tDQSQ | - | 0.4 | - | 0.4 | ns | | |
| Data-Out hold time from DQS | tQH | tHP - tQHS | - | tHP - tQHS | - | ns | 1, 10 | |
| Clock Half Period | tHP | min (tCL, tCH) | - | min (tCL, tCH) | - | ns | 1,9 | |
| Data Hold Skew Factor | tQHS | - | 0.5 | - | 0.5 | ns | 10 | |
| Data-out high-impedance window from CK, /CK | tHZ | | tAC(Max) | | tAC(Max) | ns | 17 | |
| Data-out low-impedance window from CK, /CK | tLZ | tAC(min) | tAC(Max) | tAC(min) | tAC(Max) | ns | 17 | |
| Input Setup Time (fast slew rate) | tIS | 0.6 | - | 0.6 | - | ns | 2,3,5,6 | |
| Input Hold Time (fast slew rate) | tIH | 0.6 | - | 0.6 | - | ns | 2,3,5,6 | |
| Input Setup Time (slow slew rate) | tIS | 0.7 | - | 0.7 | - | ns | 2,4,5,6 | |
| Input Hold Time (slow slew rate) | tIH | 0.7 | - | 0.7 | - | ns | 2,4,5,6 | |

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

- continued -

| Parameter | Symbol | DDR400 (D4) | | DDR400 (D43) | | Unit | Note |
|--|--------|-------------|------|--------------|------|------|------------------|
| | | Min | Max | Min | Max | | |
| Input Pulse Width | tIPW | 2.2 | - | 2.2 | - | ns | 6 |
| Write DQS High Level Width | tDQSH | 0.35 | - | 0.35 | - | CK | |
| Write DQS Low Level Width | tDQSL | 0.35 | - | 0.35 | - | CK | |
| Clock to First Rising edge of DQS-In | tDQSS | 0.72 | 1.28 | 0.72 | 1.28 | CK | |
| DQS falling edge to CK setup time | tDSS | 0.2 | | 0.2 | | CK | |
| DQS falling edge hold time from CK | tDSH | 0.2 | | 0.2 | | CK | |
| Data-In Setup Time to DQS-In (DQ & DM) | tDS | 0.4 | - | 0.4 | - | ns | 6,7,11, 12,13 |
| Data-in Hold Time to DQS-In (DQ & DM) | tDH | 0.4 | - | 0.4 | - | ns | |
| DQ & DM Input Pulse Width | tDIPW | 1.6 | - | 1.6 | - | ns | 6 |
| Read DQS Preamble Time | tRPRE | 0.9 | 1.1 | 0.9 | 1.1 | CK | |
| Read DQS Postamble Time | tRPST | 0.4 | 0.6 | 0.4 | 0.6 | CK | |
| Write DQS Preamble Setup Time | tWPRES | 0 | - | 0 | - | CK | |
| Write DQS Preamble Hold Time | tWPREH | 0.25 | - | 0.25 | - | CK | |
| Write DQS Postamble Time | tWPST | 0.4 | 0.6 | 0.4 | 0.6 | CK | |
| Mode Register Set Delay | tMRD | 2 | - | 2 | - | CK | |
| Exit self refresh to non-READ command | tXSNR | 200 | - | 200 | - | CK | 8 |
| Exit self refresh to READ command | tXSRD | 200 | - | 200 | - | CK | 8 |
| Average Periodic Refresh Interval | tREFI | - | 7.8 | - | 7.8 | us | |

Note :

1. This calculation accounts for tDQSQ(max), the pulse width distortion of on-chip circuit and jitter.
2. Data sampled at the rising edges of the clock : A0~A12, BA0~BA1, CKE, /CS, /RAS, /CAS, /WE.
3. For command/address input slew rate $\geq 1.0V/ns$
4. For command/address input slew rate $\geq 0.5V/ns$ and $< 1.0V/ns$
This derating table is used to increase tIS/tIH in case where the input slew-rate is below 0.5V/ns.
Input Setup / Hold Slew-rate Derating Table.

| Input Setup / Hold Slew-rate | Delta tIS | Delta tIH |
|------------------------------|-----------|-----------|
| V/ns | ps | ps |
| 0.5 | 0 | 0 |
| 0.4 | +50 | 0 |
| 0.3 | +100 | 0 |

5. CK, /CK slew rates are $\geq 1.0V/ns$, ie, $\geq 2.0V/ns$ differential.
6. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester correlation.
7. Data latched at both rising and falling edges of Data Strobes(LDQS/UDQS) : DQ, LDM/UDM.

8. Minimum of 200 cycles of stable input clocks after Self Refresh Exit command, where CKE is held high, is required to complete Self Refresh Exit and lock the internal DLL circuit of DDR SDRAM.
9. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).
10. tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS consists of tDQSQmax, the pulse width distortion of on-chip clock circuits, data pin to pin skew and output pattern effects and p-channel to n-channel variation of the output drivers.

11. This derating table is used to increase tDS/tDH in case where the input slew-rate is below 0.5V/ns.

Input Setup / Hold Slew-rate Derating Table.

| Input Setup / Hold Slew-rate | Delta tDS | Delta tDH |
|------------------------------|-----------|-----------|
| V/ns | ps | ps |
| 0.5 | 0 | 0 |
| 0.4 | +75 | +75 |
| 0.3 | +150 | +150 |

12. I/O Setup/Hold Plateau Derating. This derating table is used to increase tDS/tDH in case where the input level is flat below VREF +/-310mV for a duration of up to 2ns.

| I/O Input Level | Delta tDS | Delta tDH |
|-----------------|-----------|-----------|
| mV | ps | ps |
| +280 | +50 | +50 |

13. I/O Setup/Hold Delta Inverse Slew Rate Derating. This derating table is used to increase tDS/tDH in case where the DQ and DQS slew rates differ. The Delta Inverse Slew Rate is calculated as $(1/\text{SlewRate1}) - (1/\text{SlewRate2})$. For example, if slew rate 1=0.5V/ns and Slew Rate2 = 0.4V/n then the Delta Inverse Slew Rate = -0.5ns/V.

| $(1/\text{SlewRate1}) - (1/\text{SlewRate2})$ | Delta tDS | Delta tDH |
|---|-----------|-----------|
| ns/V | ps | ps |
| 0 | 0 | 0 |
| +/-0.25 | +50 | +50 |
| +/- 0.5 | +100 | +100 |

14. DQS, DM and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.
15. $tDAL = (tDPL / tCK) + (tRP / tCK)$. For each of the terms above, if not already an integer, round to the next highest integer. tCK is equal to the actual system clock cycle time.
Example: For DDR266B at CL=2.5 and tCK = 7.5 ns,
 $tDAL = (15 \text{ ns} / 7.5 \text{ ns}) + (20 \text{ ns} / 7.5 \text{ ns}) = (2.00) + (2.67)$
Round up each non-integer to the next highest integer: = (2) + (3), tDAL = 5 clock
16. For the parts which do not has internal RAS lockout circuit, Active to Read with Auto precharge delay should be tRAS - BL/2 x tCK.
17. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ), or begins driving (LZ).

SIMPLIFIED COMMAND TRUTH TABLE

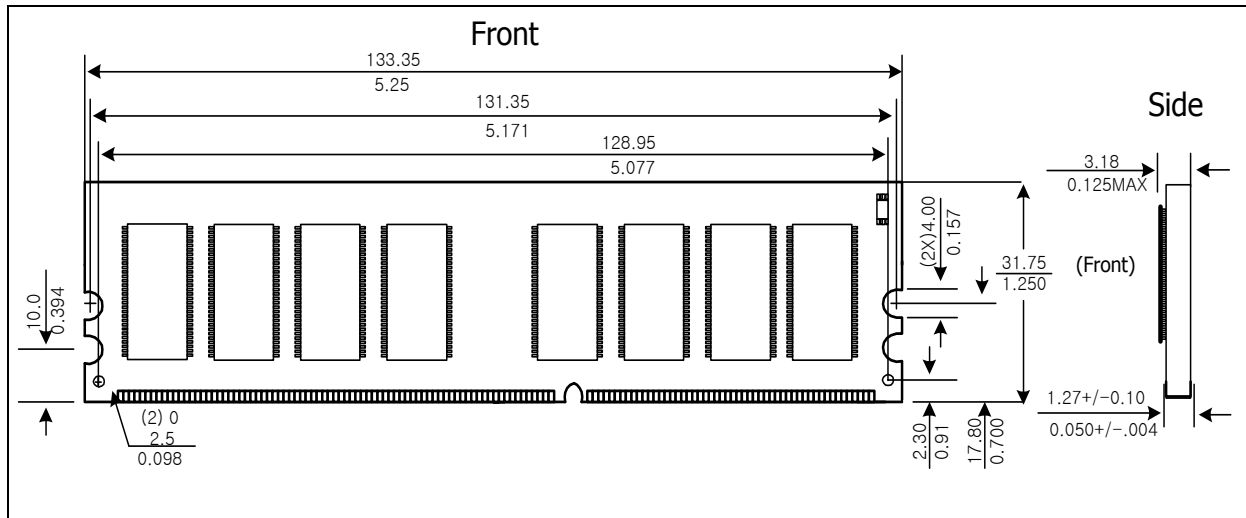
| Command | | CKEn-1 | CKEn | /CS | /RAS | /CAS | /WE | ADDR | A10/ AP | BA | Note |
|----------------------------|-------|--------|------|-----|------|------|-----|---------|------------|----|------|
| Extended Mode Register Set | | H | X | L | L | L | L | OP code | | | 1,2 |
| Mode Register Set | | H | X | L | L | L | L | OP code | | | 1,2 |
| Device Deselect | | H | X | H | X | X | X | X | | | 1 |
| No Operation | | | | L | H | H | H | | | | |
| Bank Active | | H | X | L | L | H | H | RA | | V | 1 |
| Read | | H | X | L | H | L | H | CA | L | V | 1 |
| Read with Autoprecharge | | | | | | | | | H | | 1,3 |
| Write | | H | X | L | H | L | L | CA | L | V | 1 |
| Write with Autoprecharge | | | | | | | | | H | | 1,4 |
| Precharge All Banks | | H | X | L | L | H | L | X | H | X | 1,5 |
| Precharge selected Bank | | | | | | | | | L | V | 1 |
| Read Burst Stop | | H | X | L | H | H | L | X | | | 1 |
| Auto Refresh | | H | H | L | L | L | H | X | | | 1 |
| Self Refresh | Entry | H | L | L | L | L | H | X | | | 1 |
| | Exit | L | H | H | X | X | X | | | | 1 |
| Precharge Power Down Mode | Entry | | | H | L | H | X | X | X | X | |
| | | L | H | | | H | H | 1 | | | |
| | Exit | L | H | H | X | X | X | 1 | | | |
| | | | | L | H | H | H | 1 | | | |
| Active Power Down Mode | Entry | H | L | H | X | X | X | X | | | 1 |
| | | | | L | V | V | V | | | | 1 |
| | Exit | L | H | X | | | | | | | 1 |

(H=Logic High Level, L=Logic Low Level, X=Don't Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation)

Note :

- DM states are Don't Care. Refer to below Write Mask Truth Table.
- OP Code(Operand Code) consists of A0~A12 and BA0~BA1 used for Mode Registering during Extended MRS or MRS. Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after tRP period from Precharge command.
- If a Read with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+tRP).
- If a Write with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+1+tDPL+tRP). Last Data-In to Precharge delay(tDPL) which is also called Write Recovery Time (tWR) is needed to guarantee that the last data has been completely written.
- If A10/AP is High when Row Precharge command being issued, BA0/BA1 are ignored and all banks are selected to be precharged.

PACKAGE DIMENSIONS



SPD SPECIFICATION

(32Mx64 Unbuffered DDR DIMM)

SERIAL PRESENCE DETECT

Bin Sort : J(DDR333@CL=2.5), D4/D43(DDR400@CL=3)

| Byte# | Function Description | Function Supported | | | Hexa Value | | | Note |
|-------|--|--|-----------|----------|------------|-----|-----|------|
| | | D43 | D4 | J | D43 | D4 | J | |
| 0 | Number of Bytes written into serial memory at module manufacturer | 128 Bytes | | | 80h | | | |
| 1 | Total number of Bytes in SPD device | 256 Bytes | | | 08h | | | |
| 2 | Fundamental memory type | DDR SDRAM | | | 07h | | | |
| 3 | Number of row address on this assembly | 13 | | | 0Dh | | | 1 |
| 4 | Number of column address on this assembly | 10 | | | 0Ah | | | 1 |
| 5 | Number of physical banks on DIMM | 1Bank | | | 01h | | | |
| 6 | Module data width | 64 Bits | | | 40h | | | |
| 7 | Module data width (continued) | - | | | 00h | | | |
| 8 | Module voltage Interface levels(VDDQ) | SSTL 2.5V | | | 04h | | | |
| 9 | DDR SDRAM cycle time at CAS Latency=2.5(tCK)@DDR333, 3(tCK)@DDR400 | 5.0ns | 5.0ns | 6.0ns | 50h | 50h | 60h | 2 |
| 10 | DDR SDRAM access time from clock at CL=2.5 (tAC) | +/-0.7ns | | | 70h | | | 2 |
| 11 | Module configuration type | Non-ECC | | | 00h | | | |
| 12 | Refresh rate and type | 7.8us & Self refresh | | | 82h | | | |
| 13 | Primary DDR SDRAM width | x8 | | | 08h | | | |
| 14 | Error checking DDR SDRAM data width | N/A | | | 00h | | | |
| 15 | Minimum clock delay for back-to-back random column address(tCCD) | 1 CLK | | | 01h | | | |
| 16 | Burst lengths supported | 2,4,8 | | | 0Eh | | | |
| 17 | Number of banks on each DDR SDRAM | 4 Banks | | | 04h | | | |
| 18 | CAS latency supported | 2, 2.5, 3 | 2, 2.5, 3 | 2, 2.5 | 1Ch | 1Ch | 0Ch | |
| 19 | CS latency | 0 | | | 01h | | | |
| 20 | WE latency | 1 | | | 02h | | | |
| 21 | DDR SDRAM module attributes | Differential Clock Input | | | 20h | | | |
| 22 | DDR SDRAM device attributes : General | +/-0.2Voltage tolerance, Concurrent Auto Precharge tRAS Lock Out | | | C0h | | | |
| 23 | DDR SDRAM cycle time at CL=2.0(tCK), 2.5(tCK) | 6ns | 6ns | 7.5ns | 60h | 60h | 75h | 2 |
| 24 | DDR SDRAM access time from clock at CL=2.0(tAC), 2.5(tAC) | +/-0.7ns | +/-0.7ns | +/-0.7ns | 70h | 70h | 70h | 2 |
| 25 | DDR SDRAM cycle time at CL=1.5(tCK), 2.0(tCK) | 7.5ns | 7.5ns | - | 75h | 75h | 00h | 2 |
| 26 | DDR SDRAM access time from clock at CL=1.5(tAC), 2.0(tAC) | +/-0.75ns | +/-0.75ns | - | 75h | 75h | 00h | 2 |
| 27 | Minimum row precharge time(tRP) | 15ns | 18ns | 18ns | 3Ch | 48h | 48h | |
| 28 | Minimum row activate to row active delay(tRRD) | 10ns | 10ns | 12ns | 28h | 28h | 30h | |
| 29 | Minimum RAS to CAS delay(tRCD) | 15ns | 18ns | 18ns | 3Ch | 48h | 48h | |
| 30 | Minimum active to precharge time(tRAS) | 40ns | 40n | 42ns | 28h | 28h | 2Ah | |
| 31 | Module row density | 256MB | | | 40h | | | |
| 32 | Command and address signal input setup time(tIS) | 0.6ns | 0.6ns | 0.75ns | 60h | 60h | 75h | |
| 33 | Command and address signal input hold time(tIH) | 0.6ns | 0.6ns | 0.75ns | 60h | 60h | 75h | |
| 34 | Data signal input setup time(tDS) | 0.4ns | 0.4ns | 0.45ns | 40h | 40h | 45h | |
| 35 | Data signal input hold time(tDH) | 0.4ns | 0.4ns | 0.45ns | 40h | 40h | 45h | |
| 36~40 | Reserved for VCSDRAM | Undefined | | | 00h | | | |
| 41 | Minimum active / auto-refresh time (tRC) | 55ns | 58ns | 60ns | 37h | 3Ah | 3Ch | |
| 42 | Minimum auto-refresh to active/auto-refresh command period(tRFC) | 70ns | 70ns | 72ns | 46h | 46h | 48h | |
| 43 | Maximum cycle time (tCK max) | 10ns | 10ns | 12ns | 28h | 28h | 30h | |
| 44 | Maximum DQS-DQ skew time(tDQSQ) | 0.4ns | 0.4ns | 0.45ns | 28h | 28h | 2Dh | |
| 45 | Maximum read data hold skew factor(tQHS) | 0.50ns | 0.50ns | 0.55ns | 50h | 50h | 55h | |
| 46~61 | Superset information(Reserved for IDD values, Tcase, etc.) | Undefined | | | 00h | | | |
| 62 | SPD Revision code | Initial release | | | 00h | | | |
| 63 | Checksum for Bytes 0~62 | - | | | 66h | 81h | 00h | |
| 64 | Manufacturer JEDEC ID Code | Hynix JEDEC ID | | | ADh | | | |
| 65~71 | ----- Manufacturer JEDEC ID Code | - | | | 00h | | | |

SERIAL PRESENCE DETECT
- continued -

| Byte # | Function Description | Function Supported | | | Hexa Value | | | Note |
|---------|--|---|-------|-------|--|-----|-----|------|
| | | D43 | D4 | J | D43 | D4 | J | |
| 72 | Manufacturing location | Hynix(Korea Area) HSA(United States Area) HSE(Europe Area) HSJ(Japan Area) Singapore Asia Area | | | 0'h 1'h 2'h 3'h 4'h 5'h | | | 6 |
| 73 | Manufacture part number(Hynix Memory Module) | H | | | 48h | | | |
| 74 | ----- Manufacture part number(Hynix Memory Module) | Y | | | 59h | | | |
| 75 | ----- Manufacture part number(Hynix Memory Module) | M | | | 4Dh | | | |
| 76 | Manufacture part number (DDR SDRAM) | D | | | 44h | | | |
| 77 | Manufacture part number(Memory density) | 2 | | | 32h | | | |
| 78 | Manufacture part number(Module Depth) | 3 | | | 33h | | | |
| 79 | ----- Manufacture part number(Module Depth) | 2 | | | 32h | | | |
| 80 | Manufacture part number(Module type) | Blank | | | 20h | | | |
| 81 | Manufacture part number(Data width) | 6 | | | 36h | | | |
| 82 | -----Manufacture part number(Data width) | 4 | | | 34h | | | |
| 83 | Manufacture part number(Refresh, # of Bank.) | 6(8K refresh,4Bank) | | | 36h | | | |
| 84 | Manufacture part number(Component Generation) | C | | | 43h | | | |
| 85 | Manufacture part number(Component configuration) | 8 | | | 38h | | | |
| 86 | Manufacture part number(Module Type) | J | | | 4Ah | | | |
| 87 | Manufacture part number(Hyphen) | '.' | | | 2Dh | | | |
| 88 | Manufacture part number(Minimum cycle time) | D | D | J | 44h | 44h | 4Ah | |
| 89 | Manufacture part number(Minimum cycle time) | 4 | 4 | Blank | 34h | 34h | 20h | |
| 90 | Manufacture part number(Minimum cycle time) | 3 | Blank | Blank | 33h | 20h | 20h | |
| 91 | Manufacture revision code(for Component) | - | | | - | | | |
| 92 | Manufacture revision code (for PCB) | - | | | - | | | |
| 93 | Manufacturing date(Year) | - | | | - | | | 3 |
| 94 | Manufacturing date(Week) | - | | | - | | | 3 |
| 95~98 | Module serial number | - | | | - | | | 4 |
| 99~127 | Manufacturer specific data (may be used in future) | Undefined | | | 00h | | | 5 |
| 128~255 | Open for customer use | Undefined | | | 00h | | | 5 |

Note :

1. The bank address is excluded
2. These value is based on the component specification
3. These bytes are programmed by code of date week & date year
4. These bytes apply to Hynix's own Module Serial Number system
5. These bytes undefined and coded as '00h'
6. Refer to Hynix web site